

REPETITIVE AVALANCHE AND dv/dt RATED HEXFET® TRANSISTOR

IRHNA7Z60 IRHNA8Z60 N-CHANNEL MEGA RAD HARD

30 Volt, 0.009W, RAD HARD HEXFET

International Rectifier's RAD HARD technology HEXFETs demonstrate immunity to SEE failure. Additionally, under **identical** pre- and post-irradiation test conditions, International Rectifier's RAD HARD HEXFETs retain **identical** electrical specifications up to 1×10^5 Rads (Si) total dose. No compensation in gate drive circuitry is required. These devices are also capable of surviving transient ionization pulses as high as 1×10^{12} Rads (Si)/Sec, and return to normal operation within a few microseconds. Since the RAD HARD process utilizes International Rectifier's patented HEXFET technology, the user can expect the highest quality and reliability in the industry.

RAD HARD HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high-energy pulse circuits in space and weapons environments.

Product Summary

Part Number	BV _{DSS}	R _{DS(on)}	I _D
IRHNA7Z60	30V	0.009W	75*A
IRHNA8Z60	30V	0.009W	75*A

Features:

- Radiation Hardened up to 1×10^6 Rads (Si)
- Single Event Burnout (SEB) Hardened
- Single Event Gate Rupture (SEGR) Hardened
- Gamma Dot (Flash X-Ray) Hardened
- Neutron Tolerant
- Identical Pre- and Post-Electrical Test Conditions
- Repetitive Avalanche Rating
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- LightWeight

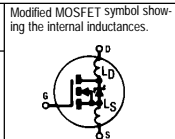
Absolute Maximum Ratings

Pre-Irradiation

	Parameter	IRHNA7Z60, IRHNA8Z60	Units
I _D @ V _{GS} = -12V, T _C = 25°C	Continuous Drain Current	75*	A
I _D @ V _{GS} = -12V, T _C = 100°C	Continuous Drain Current	75*	
I _{DM}	Pulsed Drain Current ①	300	
P _D @ T _C = 25°C	Max. Power Dissipation	300	W
	Linear Derating Factor	2.4	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
EAS	Single Pulse Avalanche Energy ②	500	mJ
I _{AR}	Avalanche Current ①	75	A
EAR	Repetitive Avalanche Energy ①	30	mJ
dv/dt	Peak Diode Recovery dv/dt ③	0.35	V/ns
T _J	Operating Junction	-55 to 150	°C
T _{STG}	Storage Temperature Range		
	Package Mounting surface Temperature	300 (for 5 sec.)	
	Weight	3.3 (typical)	g

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V _{GS} = 0V, I _D = 1.0mA
dBV _{DSS} /dT _J	Temperature Coefficient of Breakdown Voltage	—	0.023	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.009		V _{GS} = 12V, I _D = 75A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 1.0mA
g _{fs}	Forward Transconductance	31	—	—	S (M)	V _{DS} > 15V, I _{DS} = 75A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	25	mA	V _{DS} = 0.8 x Max Rating, V _{GS} = 0V
		—	—	250		V _{DS} = 0.8 x Max Rating V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	421	nC	V _{GS} = 12V, I _D = 75A
Q _{gs}	Gate-to-Source Charge	—	—	104		V _{DS} = Max Rating x 0.5
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	74		
t _{d(on)}	Turn-On Delay Time	—	—	32	ns	V _{DD} = 15V, I _D = 75A, R _G = 2.35Ω
t _r	Rise Time	—	—	370		
t _{d(off)}	Turn-Off Delay Time	—	—	150		
t _f	Fall Time	—	—	280		
L _D	Internal Drain Inductance	—	0.8	—	nH	Measured from drain lead, 6mm (0.25 in) from package to center of die.
L _S	Internal Source Inductance	—	2.8	—		Measured from source lead, 6mm (0.25 in) from package to source bonding pad.
C _{iss}	Input Capacitance	—	7000	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	4800	—		
C _{rss}	Reverse Transfer Capacitance	—	1800	—		



Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	75*	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier.
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	300		
V _{SD}	Diode Forward Voltage	—	—	1.8	V	T _j = 25°C, I _S = 75A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	245	ns	T _j = 25°C, I _F = 75A, di/dt ≤ 100A/ms
Q _{RR}	Reverse Recovery Charge	—	—	1.1	mC	V _{DD} ≤ 50V ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				



Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	0.42	°C/W	Soldered to a 1 inch square clad PC board
R _{thJ-PCB}	Junction-to-PC board	—	1.6	—		

* Current is limited by internal wire diameter (Die current is 75A , see page 6)

Radiation Performance of Rad Hard HEXFETs

International Rectifier Radiation Hardened HEXFETs are tested to verify their hardness capability. The hardness assurance program at International Rectifier comprises three radiation environments.

Every manufacturing lot is tested in a low dose rate (total dose) environment per MIL-STD-750, test method 1019 condition A. International Rectifier has imposed a standard gate condition of 12 volts per note 5 and a V_{DS} bias condition equal to 80% of the device rated voltage per note 6. Pre- and post- irradiation limits of the devices irradiated to 1×10^5 Rads (Si) are identical and are presented in Table 1, column 1, IRHNA7Z60. Post-irradiation limits of the devices irradiated to 1×10^6 Rads (Si) are presented in Table 1, column 2,

IRHNA8Z60. The values in Table 1 will be met for either of the two low dose rate test circuits that are used. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

High dose rate testing may be done on a special request basis using a dose rate up to 1×10^{12} Rads (Si)/Sec (See Table 2).

International Rectifier radiation hardened HEXFETs have been characterized in heavy ion Single Event Effects (SEE) environments. Single Event Effects characterization is shown in Table 3.

Table 1. Low Dose Rate ⑤ ⑥

Parameter	Description	IRHNA7Z60		IRHNA8Z60		Units	Test Conditions ⑧
		100K Rads (Si)		1000K Rads (Si)			
		Min	Max	Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	—	30	—	V	$V_{GS} = 0V, I_D = 1.0mA$
$V_{GS(th)}$	Gate Threshold Voltage ④	2.0	4.0	1.25	4.5		$V_{GS} = V_{DS}, I_D = 1.0mA$
I_{GSS}	Gate-to-Source Leakage Forward	—	100	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100	—	-100		$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	25	—	50	μA	$V_{DS}=0.8 \times \text{Max Rating}, V_{GS} = 0V$
$R_{DS(on)1}$	Static Drain-to-Source On-State Resistance One ④	—	.009	—	.03	ω	$V_{GS} = 12V, I_D = 15A$
V_{SD}	Diode Forward Voltage ④	—	1.8	—	1.8	V	$T_C = 25^\circ C, I_S = 15A, V_{GS} = 0V$

Table 2. High Dose Rate ⑦

Parameter	Description	10^{11} Rads (Si)/sec			10^{12} Rads (Si)/sec			Units	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
V_{DSS}	Drain-to-Source Voltage	—	—	24	—	—	24	V	Applied drain-to-source voltage during gamma-dot
I_{PP}	Peak radiation induced photo-current	—	140	—	—	140	—	A	Peak radiation induced photo-current
di/dt	Rate of rise of photo-current	—	800	—	—	160	—	A/ μ sec	Rate of rise of photo-current
L_1	Circuit inductance required to limit di/dt	0.1	—	—	0.8	—	—	μH	Circuit inductance required to limit di/dt

Table 3. Single Event Effects

Ion	LET (Si) (MeV/mg/cm ²)	Fluence (ions/cm ²)	Range (μm)	V_{DS} Bias (V)	V_{GS} Bias (V)
Cu	28	3×10^5	43	26	-5

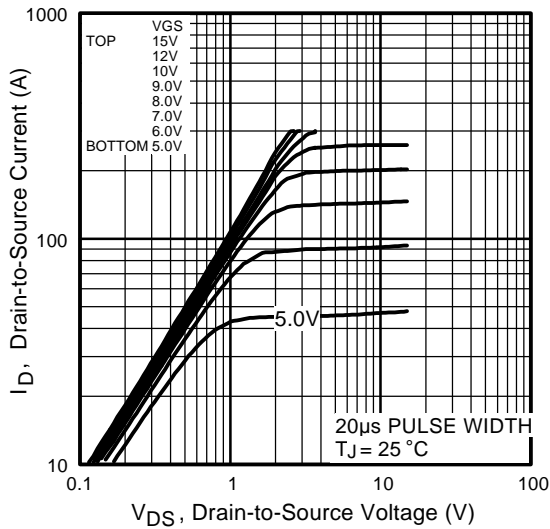


Fig 1. Typical Output Characteristics

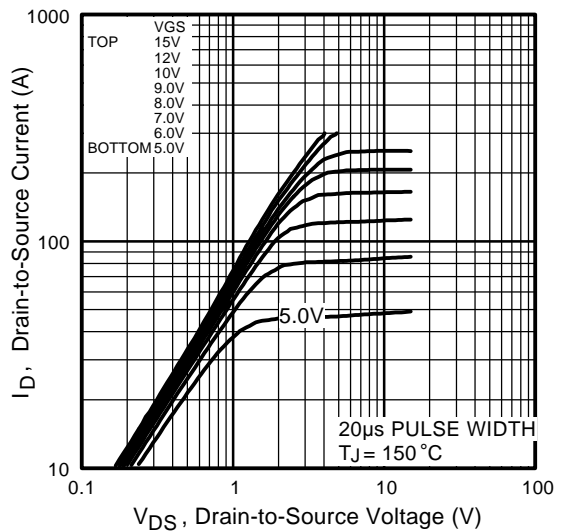


Fig 2. Typical Output Characteristics

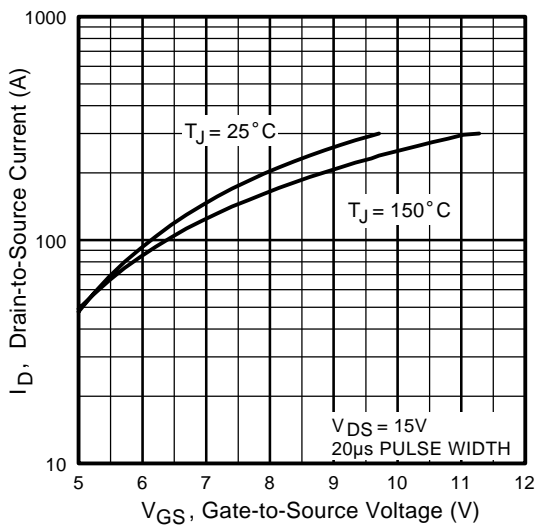


Fig 3. Typical Transfer Characteristics

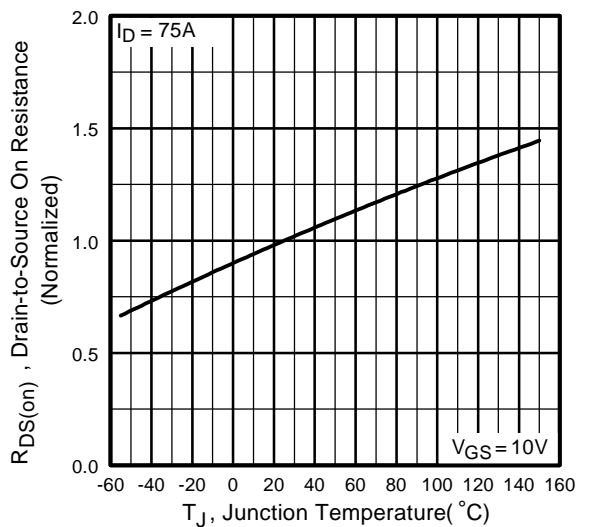


Fig 4. Normalized On-Resistance Vs. Temperature

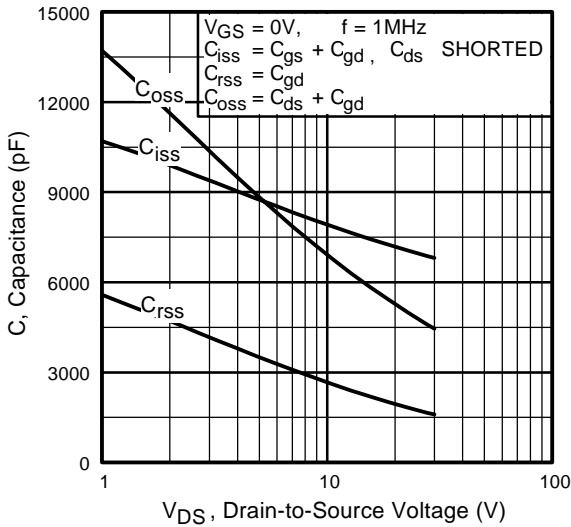


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

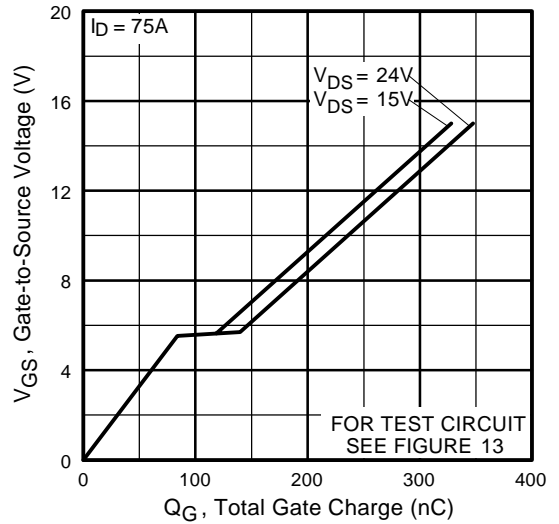


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

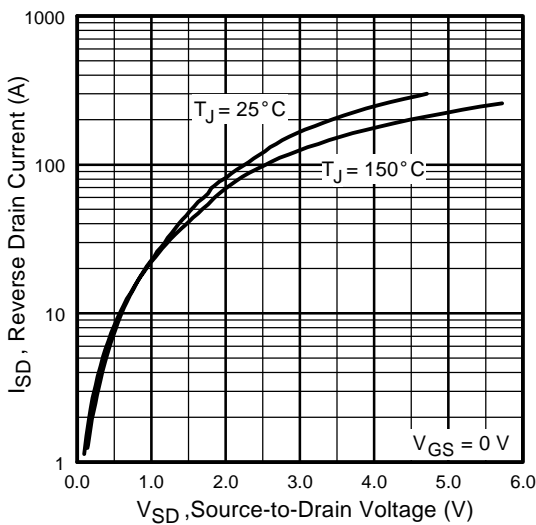


Fig 7. Typical Source-Drain Diode Forward Voltage

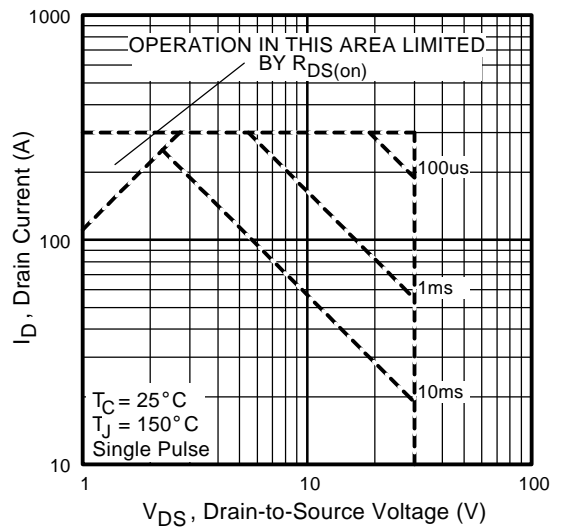


Fig 8. Maximum Safe Operating Area

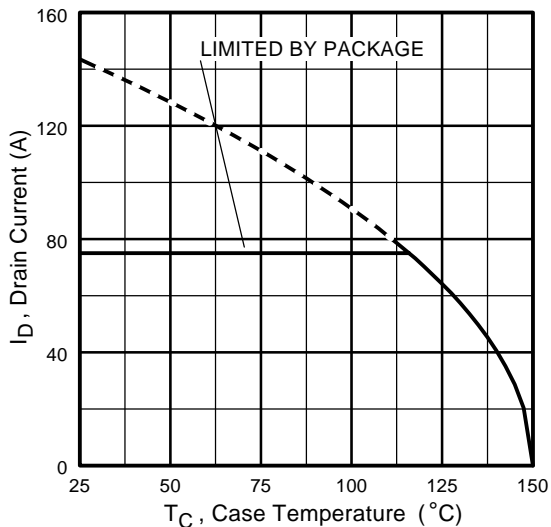


Fig 9. Maximum Drain Current Vs. Case Temperature

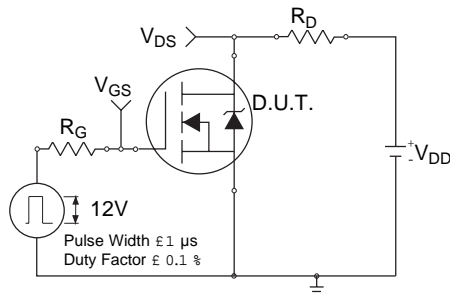


Fig 10a. Switching Time Test Circuit

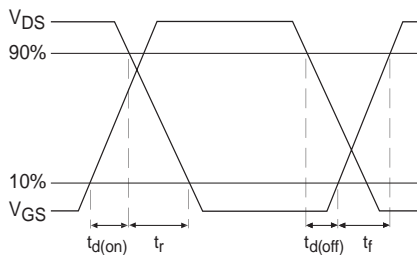


Fig 10b. Switching Time Waveforms

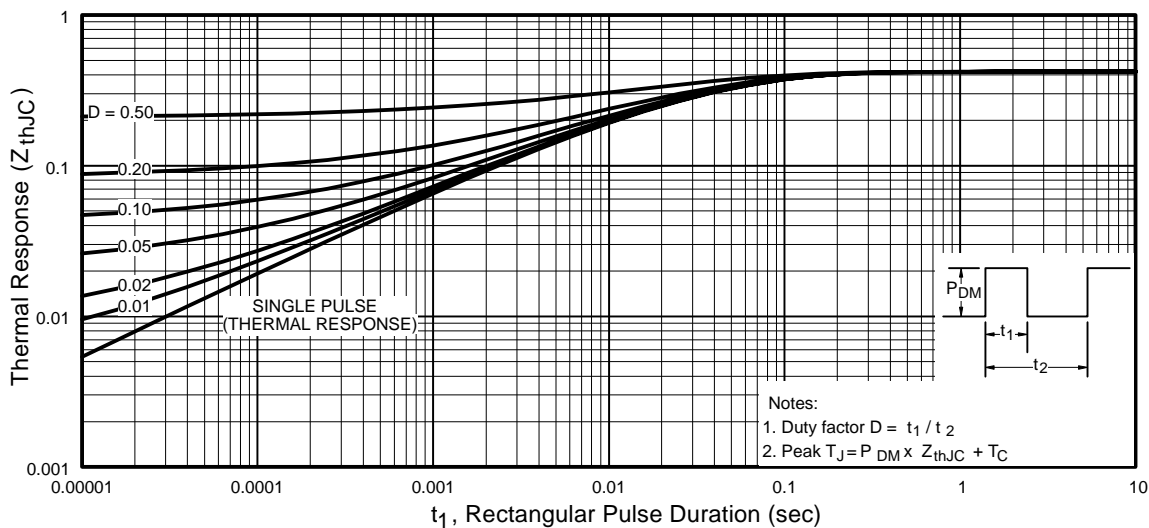


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

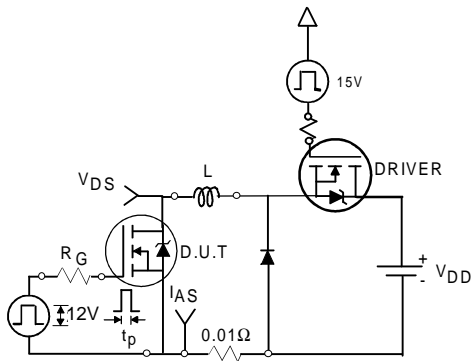


Fig 12a. Unclamped Inductive Test Circuit

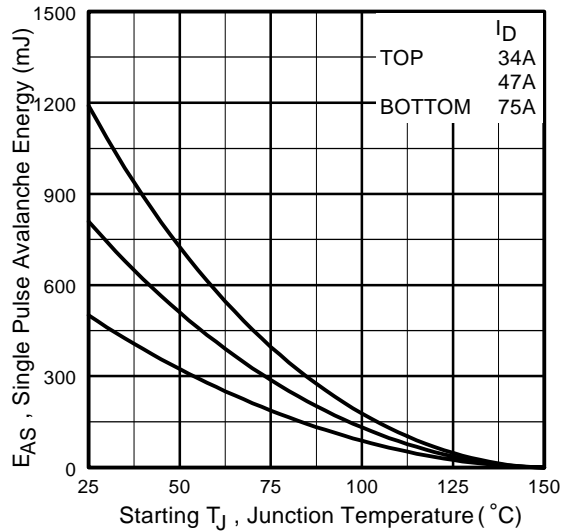


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

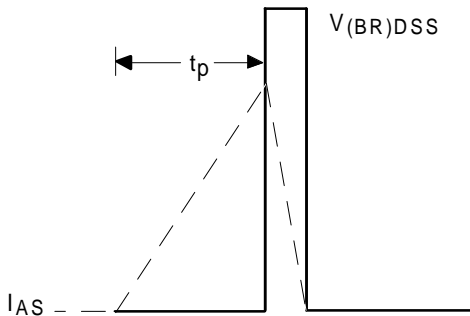


Fig 12b. Unclamped Inductive Waveforms

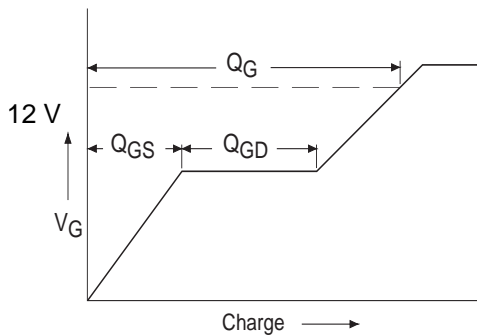


Fig 13a. Basic Gate Charge Waveform

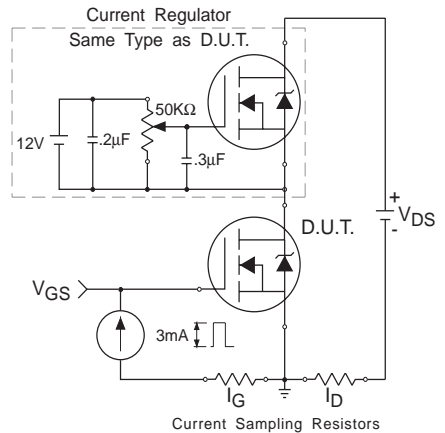
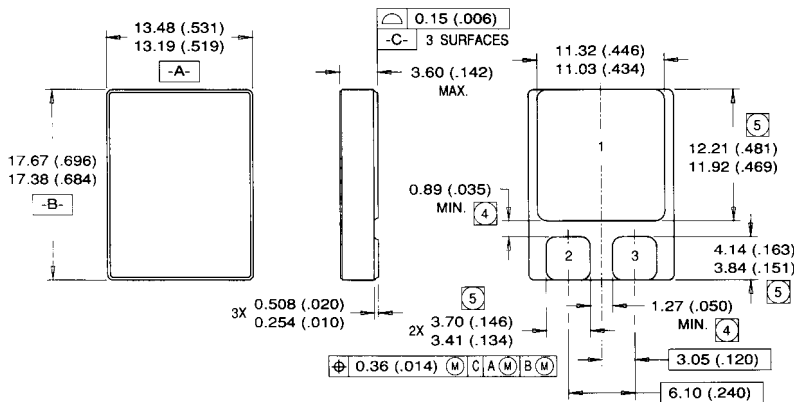


Fig 13b. Gate Charge Test Circuit

- ① Repetitive Rating; Pulse width limited by maximum junction temperature. Refer to current HEXFET reliability report.
- ② $V_{DD} = 25V$, starting $T_J = 25^\circ C$, $E_{AS} = [0.5 * L * (I_L^2)]$
Peak $I_L = 75A$, $V_{GS} = 12V$
- ③ $I_{SD} \leq 75A$, $di/dt \leq 94A/ms$,
 $V_{DD} \leq BV_{DSS}$, $T_J \leq 150^\circ C$
Suggested $RG = 0 \Omega$
- ④ Pulse width $\leq 300 ms$; Duty Cycle $\leq 2\%$
- ⑤ **Total Dose Irradiation with V_{GS} Bias.**
12 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.**
 $V_{DS} = 0.8$ rated BV_{DSS} (pre-irradiation) applied and $V_{GS} = 0$ during irradiation per MIL-STD -750, method 1019, condition A.
- ⑦ This test is performed using a flash x-ray source operated in the e-beam mode (energy ~2.5 MeV), 30 nsec pulse.
- ⑧ All Pre-Irradiation and Post-Irradiation test conditions are **identical** to facilitate direct comparison for circuit applications.

Case Outline and Dimensions — SMD-2



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
- ④ DIMENSION INCLUDES METALLIZATION FLASH.
- ⑤ DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

LEAD ASSIGNMENTS

- 1 = DRAIN
- 2 = GATE
- 3 = SOURCE

SMD-2

International
IOR Rectifier

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